

Overview

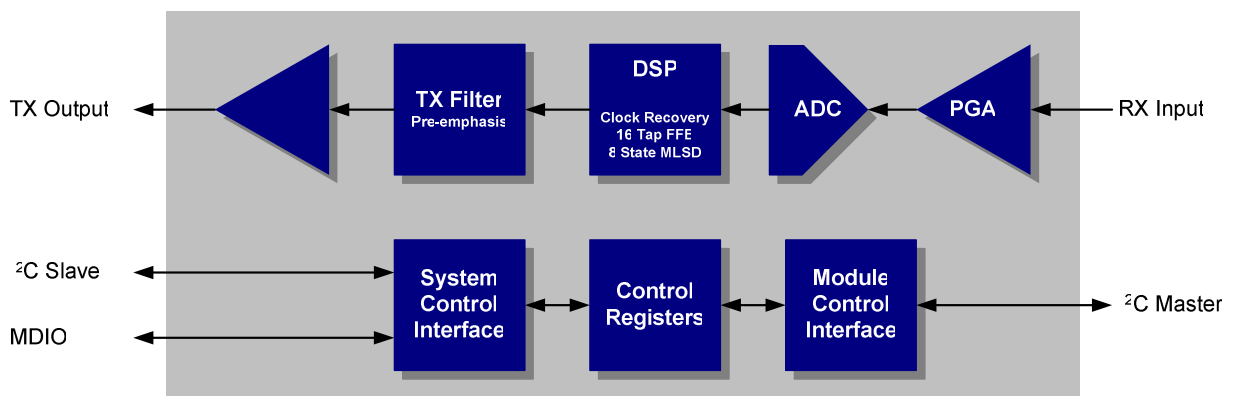
ClariPhy Communications' CL1012 is a 9.9 - 11.4 Gbit/s repeater/retimer IC combining Clock and Data Recovery (CDR) with all-digital electronic dispersion compensation (EDC). The CL1012 supports SONET/SDH transmission over single mode fiber at distances up to 100s of kilometers without optical dispersion compensation. It also supports all serial 10G Ethernet standards for multimode fiber, single mode fiber and twinax copper cable. Its all-digital EDC engine uses the optimal maximum likelihood sequence detection (MLSD) algorithm, providing robust tolerance to chromatic dispersion (CD), polarization mode dispersion (PMD) and/or modal dispersion, and enabling best in class link budget margin. Functional blocks include Maximum Likelihood Sequence Detection (MLSD), Feed Forward Equalization (FFE), Transmit Pre-emphasis, and Clock and Data Recovery (CDR). Applications include 300 pin MSA transponders as well as XFP and XFPe transceivers.

Key Features

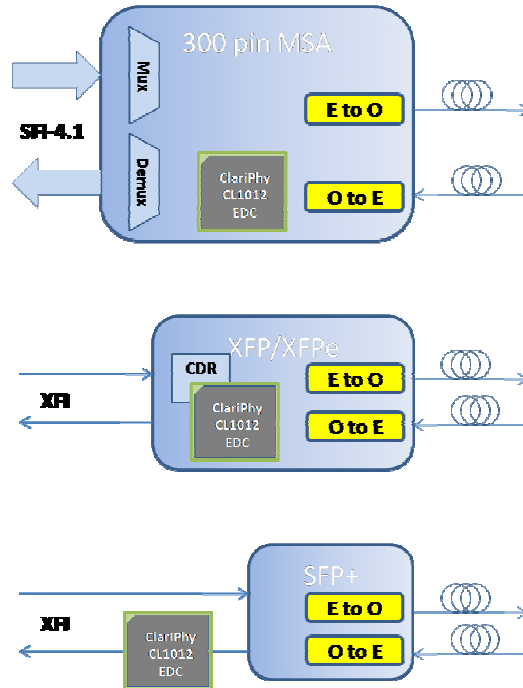
- Universal CDR with built-in EDC for metro, and long-haul SONET/SDH and DWDM applications
- Single-chip CMOS with integrated ADC and DSP
- 16-tap FFE and 8-state MLSD
- Operates at data rates from 9.9 to 11.4G
- Offset threshold adjustment for ASE noise
- Built-in pattern generators (PRBS9/31) and BER detectors
- On board channel diagnostics
- MDIO and I²C Management Interfaces
- 10x10 mm², 144 BGA Package

Major Benefits

- All-digital MLSD-based EDC offers robust compensation of CD, PMD and nonlinearities
- Small footprint for 300 pin, XFPe, XFP MSA applications
- Integrated CMOS implementation behaves reliably and robustly across voltage and temperature
- DSP-based timing recovery and adaptation guarantees predictable and consistent convergence
- DSP provides multiple diagnostic and self-test features



Application Diagrams



Application Diagrams

For more information on ClariPhy's products please visit our website www.clariphy.com or contact us at info@clariphy.com.